Amendments to the Specification

Please replace the paragraph that starts on page 8, line 19 and continues through page 9, line 3, to read as follows:

Thus, in one aspect, the present invention provides a game system comprising a Central Processing Unit (CPU) operatively connected to an external memory, one or more peripherals, and a Physics Processing Unit (PPU). The PPU is preferably a separate chip designed to efficiently provide physics simulation data and communicate this data to the CPU. The PPU may be viewed in this aspect much like a Graphics Processing Unit (GPU). GPUs are typically separate co-processors designed to efficiently render graphics data from a CPU. In a related aspect, the present invention fully contemplates the combination of a PPU with a GPU within a game system. This combination of PPU and GPU may take [[to]] the form of two chips on a single board or a single chip implementing both PPU and GPU functionality.

Please replace the paragraph that starts on page 9, line 11, to read as follows:

In a more detailed and exemplary aspect of the ~~resent~~ present invention, the PPU includes a PPU Control Engine (PCE) controlling the operation of the PPU and communication of physics simulation data with the host. The PPU also includes a Data Movement Engine (DME) responsive to commands received from the PCE and executing programs adapted to perform data movement operations. The PPU also includes a Floating Point Engine (FPE), responsive to commands from the DME and executing floating point calculations. A high-speed data bus is preferably provided to connect a high-speed memory to the DME and FPE.

Please replace the paragraph that starts on page 10, line 10, to read as follows:

Thus, in another aspect, the present invention provides a hardware-based PPU connected to a host CPU via a physical interface. The stand alone (i.e., separate chip)

PPU comprises the PCE, DME, and FPE and is described in the exemplary embodiment that follows.

Please replace the paragraph that starts on page 14, line 16, and continues through page 15, line 2, to read as follows:

Physical incorporation of PPU 16 into a PC may be accomplished using one of several approaches. First, a PPU[[s]] may be incorporated using a standard PC Interface (PCI) card optionally inserted within the PC. Alternatively, a PCI-Express Interface card might be used. A USB2 or Firewire connection to an externally packaged PPU module might be used instead of a internally configured interface card. It is readily foreseeable that a PPU and a GPU will be combined on a single interface card. That is, both chips will be physically mounted on the same card (AGP or PCI-Express), but not directly interfaced with one another. Ultimately, a single interface card having a directly interfaced PPU-GPU combination is expected, but such a combination is probably a generation away. So too is a combination within a single chip of PPU and GPU functionalities.

Please replace the paragraph that starts on page 15, line 12, to read as follows:

In addition to game engine 21 and GPU driver 23, and their associated APIs, the present invention provides a PPU driver 24 with an associated API. PPU operation is directed through the PPU driver by at least game program 20. With this arrangement, game physics are principally (if not solely) implemented in a dedicated hardware device designed specifically to provide physics simulation data. This contrasts sharply with the conventional approach of implementing physics completely in software run on the general purpose CPU.

Please replace the paragraph that starts on page 16, line 14, and continues through page 17, line 2, to read as follows:

The exemplary PPU architectures shown in Figures 3-5 are shown in some additional detail beginning with Figure 6. The various elements described below connect to a peripheral bus 40 and processor bus 44 to form a processor architecture similar to conventional embedded system on a chip (SOC) designs. Within this expanded architecture, processor bus 44 is respectively connected with peripheral bus 40 and high-speed data bus (HSB) 48 via conventional bus bridges 43 and 47. Peripheral bus 40 allows connection of the PPU to general I/Os 30 and UART 31, as examples, using a peripheral bus arbitration circuit 41 and timer circuit 42. Processor bus 44 facilitates connection of the PPU to a host (a PC or stand alone game console) via one or more physical interfaces, such as PCI interface 34, USB2 controller 35, and/or an IEEE 1394 Firewire Interface. The RISC [[cores]] core forming PPU Control Engine (PCE) 17 also connects to processor bus 44, along with a processor bus arbitration circuit 45 and DMA controller 46. A DCQ/DRQ circuit 56 connects processor bus 44 directly with Data Movement Engine (DME) 18.